

**CLAIMS**

What is claimed is:

1           1.     An electronic circuit for controlling electron beams from a plurality of  
2     field emission cathodes to produce a color image from a television signal onto a phosphor  
3     screen of a cathode ray tube (CRT), comprising:

4           a video memory adapted to receive and store color video information from a  
5     video source, the color video information comprising red, green and blue intensity values  
6     for each spot to be illuminated on a cathode ray tube (CRT) having a plurality of  
7     substantially vertical red, green and blue phosphor stripes, wherein adjacent portions of  
8     the red, green and blue phosphor stripes comprise the spots to be illuminated;

9           the video memory having addressable first, second and third memory portions for  
10    storing the red, green and blue intensity values, respectively, wherein the red, green and  
11    blue intensity values for a spot are stored at the same corresponding address of the first,  
12    second and third memory portions, respectively;

13          an address counter for selecting memory addresses corresponding to spot  
14    locations on the CRT face, the address counter coupled to the video memory;

15          a color multiplexer having first, second and third inputs coupled to the first,  
16    second and third memory portions, respectively, and an output;

17          a color counter coupled to and controlling the color multiplexer for selecting the  
18    red, green and blue intensity values from the video memory, wherein the color counter  
19    increments the address counter after each selection sequence of red, green and blue  
20    intensity values;

21 a gate multiplexer have a first input, a second input and an output, the gate  
22 multiplexer first input coupled to the color multiplexer output, and the gate multiplexer  
23 second input set to a zero intensity value;

24 a phase counter coupled to and controlling the gate multiplexer, wherein the phase  
25 counter switches the gate multiplexer output to the second input having the zero intensity  
26 value at each fourth phase count;

27 an intensity value shift register adapted for receiving intensity values from the  
28 gate multiplexer and storing the received intensity values in sequential order, the intensity  
29 value shift register comprising a plurality of registers, wherein an input of a first one of  
30 the plurality of registers is connected to the output of the gate multiplexer and remaining  
31 ones of the plurality of registers each have an output connected to an input of a  
32 subsequent one until the subsequent one is a last one of the plurality of registers;

33 a plurality of digital-to-analog converters (DACs), each of the plurality of DACs  
34 having an output adapted for coupling to a respective one of a plurality of field emission  
35 cathodes;

36 a first one of the plurality of DACs having an input coupled to the output of the  
37 gate multiplexer, and an input of each of the remaining ones of the plurality of DACs  
38 being connected to the output of respective ones of the plurality of registers; and

39 a video clock having an output coupled to the phase counter and the intensity  
40 value shift register, wherein the video clock times when the red, green and blue intensity  
41 values for each spot and the zero intensity value between adjacent spots are applied  
42 through the plurality of field emission cathodes to the spot portions of the phosphor  
43 stripes of the CRT.

1           2.       The apparatus of claim 1, wherein each of the plurality of registers can store an  
2   eight bit intensity value.

1           3.       The apparatus of claim 1, further comprising:  
2                   first, second and third multipliers for gamma correcting the red, green and blue  
3   intensity values, respectively; and  
4                   the first, second and third multipliers coupled between the first, second and third  
5   memory portions and the first, second and third inputs of the color multiplexer.

1           4.       The apparatus of claim 1, wherein the number of the plurality of DACs is selected  
2   from the group consisting of 2, 3, 4, 5, 6, 7, 8, 9 and 10.

1           5.       The apparatus of claim 1, wherein the number of the plurality of registers is  
2   selected from the group consisting of 2, 3, 4, 5, 6, 7, 8, 9 and 10.

1           6.       An electronic circuit for controlling electron beams from a plurality of field  
2   emission cathodes to produce a color image from a television signal onto a phosphor screen of a  
3   cathode ray tube (CRT), comprising:  
4                   a color multiplexer adapted for receiving color video information comprising red,  
5   green and blue intensity values, the color multiplexer having first, second and third inputs  
6   adapted for receiving the red, green and blue intensity values, respectively;  
7                   a color counter coupled to and controlling the color multiplexer for selecting the  
8   red, green and blue intensity values;

9 a gate multiplexer have a first input, a second input and an output, the gate  
10 multiplexer first input coupled to the color multiplexer output, and the gate multiplexer  
11 second input set to a zero intensity value;

12 a phase counter coupled to and controlling the gate multiplexer, wherein the phase  
13 counter switches the gate multiplexer output to the second input having the zero intensity  
14 value at each fourth phase count;

15 an intensity value shift register adapted for receiving intensity values from the  
16 gate multiplexer and storing the received intensity values in sequential order, the intensity  
17 value shift register comprising a plurality of registers, wherein an input of a first one of  
18 the plurality of registers is connected to the output of the gate multiplexer and remaining  
19 ones of the plurality of registers each have an output connected to an input of a  
20 subsequent one until the subsequent one is a last one of the plurality of registers;

21 a plurality of digital-to-analog converters (DACs), each of the plurality of DACs  
22 having an output adapted for coupling to a respective one of a plurality of field emission  
23 cathodes;

24 a first one of the plurality of DACs having an input coupled to the output of the  
25 gate multiplexer, and an input of each of the remaining ones of the plurality of DACs  
26 being connected to the output of respective ones of the plurality of registers; and

27 a video clock having an output coupled to the phase counter and the intensity  
28 value shift register, wherein the video clock times when the red, green and blue intensity  
29 values for each spot and the zero intensity value between adjacent spots are applied  
30 through the plurality of field emission cathodes to the spot portions of the phosphor  
31 stripes of the CRT.

1           7.     The apparatus of claim 6, wherein each of the plurality of registers can store an  
2 eight bit intensity value.

1           8.     A method for controlling electron beams from a plurality of field emission  
2 cathodes to produce a color image from a television signal onto a phosphor screen of a cathode  
3 ray tube (CRT), the method comprising the steps of:

4                 providing a video memory adapted to receive and store color video information  
5 from a video source, the color video information comprising red, green and blue intensity  
6 values for each spot to be illuminated on a cathode ray tube (CRT) having a plurality of  
7 substantially vertical red, green and blue phosphor stripes, wherein adjacent portions of  
8 the red, green and blue phosphor stripes comprise the spots to be illuminated;

9                 storing the red, green and blue intensity values into first, second and third  
10 addressable memory portions, respectively, of the video memory;

11                selecting memory addresses corresponding to spot locations on the CRT face with  
12 an address counter;

13                providing a color multiplexer having first, second and third inputs coupled to the  
14 first, second and third memory portions, respectively, and an output;

15                selecting the red, green and blue intensity values from the video memory with a  
16 color counter coupled to and controlling the color multiplexer, wherein the color counter  
17 increments the address counter after each selection sequence of red, green and blue  
18 intensity values;

19                providing a gate multiplexer have a first input, a second input and an output, the  
20 gate multiplexer first input coupled to the color multiplexer output, and the gate  
21 multiplexer second input set to a zero intensity value;

22 providing a phase counter coupled to and controlling the gate multiplexer,  
23 wherein the phase counter switches the gate multiplexer output to the second input  
24 having the zero intensity value at each fourth phase count;

25 providing an intensity value shift register adapted for receiving intensity values  
26 from the gate multiplexer and storing the received intensity values in sequential order, the  
27 intensity value shift register comprising a plurality of registers, wherein an input of a first  
28 one of the plurality of registers is connected to the output of the gate multiplexer and  
29 remaining ones of the plurality of registers each have an output connected to an input of a  
30 subsequent one until the subsequent one is a last one of the plurality of registers;

31 providing a plurality of digital-to-analog converters (DACs), each of the plurality  
32 of DACs having an output adapted for coupling to a respective one of a plurality of field  
33 emission cathodes;

34 wherein a first one of the plurality of DACs having an input coupled to the output  
35 of the gate multiplexer, and an input of each of the remaining ones of the plurality of  
36 DACs being connected to the output of respective ones of the plurality of registers; and

37 providing a video clock having an output coupled to the phase counter and the  
38 intensity value shift register, wherein the video clock times when the red, green and blue  
39 intensity values for each spot and the zero intensity value between adjacent spots are  
40 applied through the plurality of field emission cathodes to the spot portions of the  
41 phosphor stripes of the CRT.

1 9. A system having an electronic circuit for controlling electron beams from a  
2 plurality of field emission cathodes to produce a color image from a television signal onto a  
3 phosphor screen of a cathode ray tube (CRT), the system comprising:

4           a video memory for receiving and storing color video information from a video  
5           source, the color video information comprising red, green and blue intensity values for  
6           each spot to be illuminated on a cathode ray tube (CRT) having a plurality of  
7           substantially vertical red, green and blue phosphor stripes, wherein adjacent portions of  
8           the red, green and blue phosphor stripes comprise the spots to be illuminated;

9           the video memory having addressable first, second and third memory portions for  
10          storing the red, green and blue intensity values, respectively, wherein the red, green and  
11          blue intensity values for a spot are stored at the same corresponding address of the first,  
12          second and third memory portions, respectively;

13          an address counter for selecting memory addresses corresponding to spot  
14          locations on the CRT face, the address counter coupled to the video memory;

15          a color multiplexer having first, second and third inputs coupled to the first,  
16          second and third memory portions, respectively, and an output;

17          a color counter coupled to and controlling the color multiplexer for selecting the  
18          red, green and blue intensity values from the video memory, wherein the color counter  
19          increments the address counter after each selection sequence of red, green and blue  
20          intensity values;

21          a gate multiplexer have a first input, a second input and an output, the gate  
22          multiplexer first input coupled to the color multiplexer output, and the gate multiplexer  
23          second input set to a zero intensity value;

24          a phase counter coupled to and controlling the gate multiplexer, wherein the phase  
25          counter switches the gate multiplexer output to the second input having the zero intensity  
26          value at each fourth phase count;

an intensity value shift register adapted for receiving intensity values from the gate multiplexer and storing the received intensity values in sequential order, the intensity value shift register comprising a plurality of registers, wherein an input of a first one of the plurality of registers is connected to the output of the gate multiplexer and remaining ones of the plurality of registers each have an output connected to an input of a subsequent one until the subsequent one is a last one of the plurality of registers;

a plurality of digital-to-analog converters (DACs), each of the plurality of DACs having an output coupled to a respective one of a plurality of field emission cathodes;

a first one of the plurality of DACs having an input coupled to the output of the gate multiplexer, and an input of each of the remaining ones of the plurality of DACs being connected to the output of respective ones of the plurality of registers; and

a video clock having an output coupled to the phase counter and the intensity value shift register, wherein the video clock times when the red, green and blue intensity values for each spot and the zero intensity value between adjacent spots are applied through the plurality of field emission cathodes to the spot portions of the phosphor stripes of the CRT.

10. The system of claim 9, wherein each of the plurality of registers can store an eight bit intensity value.



1           11.    The system of claim 9, further comprising:  
2                   first, second and third multipliers for gamma correcting the red, green and blue  
3           intensity values, respectively; and  
4                   the first, second and third multipliers coupled between the first, second and third  
5           memory portions and the first, second and third inputs of the color multiplexer.

1           12.    The system of claim 9, wherein the number of the plurality of DACs is selected  
2    from the group consisting of 2, 3, 4, 5, 6, 7, 8, 9 and 10.

1           13.    The system of claim 9, wherein the number of the plurality of registers is selected  
2    from the group consisting of 2, 3, 4, 5, 6, 7, 8, 9 and 10.